AMD

Using the Am79C874 NetPHY™-1LP Device to Replace the TDK 78Q2120

Application Note

Using the Am79C874 NetPHY™-1LP Device to Replace the TDK 78Q2120

Application Note

This application note provides a description of how to replace the TDK 78Q2120 with the AMD Am79C874 NetPHY-1LP device. Also, it provides a brief comparison of the functionality of the two devices, along with a detailed pin-by-pin comparison. And lastly, it provides a description of the replacement or elimination of external passive components.

PRODUCT COMPARISON

Table 1 is a comparison of Am79C874 NetPHY-1LP features and TDK 78Q2120 features.

Table 1. Feature Comparison

Feature	78Q2120	NetPHY-1LP
Power Supply	5 V or 3.3 V	Single 3.3 V (5V tolerant I/O)
Package	80-lead TQFP	80-lead TQFP
Typical Power	313 mW at 3.3 V 525 mW at 5 V	325 mW
10BASE-T	Yes	Yes
10BASE-TX	Yes	Yes
10BASE-FX	No	Yes
MII	Yes	Yes
GPSI (7-Wire)	No	Yes
5B Symbol (PCS Bypass)	Yes	Yes
LED Support	Link, TX, RX, COL, Speed, Duplex	Link, TX, RX, COL, Speed, Duplex, Advanced LED Mode (Bicolor options)
Magnetics	1:1	1:1 or 1.25:1
Internal Pull up/ Pull down	No	Yes

Pin Comparison

The TDK 78Q2120 and the AMD Am79C874 NetPHY-1LP device are generally pin-for-pin replacements. The NetPHY-1LP device includes additional functionality, beyond that of the 78Q2120. The NetPHY-1LP device can also be operated with a 1.25:1 transformer to further reduce power in the transmit section. In Table 2, the two devices are compared, pin by pin. Where there are differences between the functions of the equivalent pins, those differences are described in the comments.

Notes:

1. *Blank comment lines Table 2 indicate that the pin functions are identical.*
2. *Differences listed in the comments are all additional functions that the NetPHY-1LP device includes, beyond those incorporated in the 78Q2120.*
3. *The NetPHY-1LP device may be placed in an existing 78Q2120 design and will function equivalently to the 78Q2120, with only minor changes to the RIBB and RIBB_RET pins.*

Publication# **22941** Rev: **B** Amendment/**0**
Issue Date: **June 2000**

Table 2. NetPHY-1LP and 78Q2120 Functionally Equivalent Pins

Pin Number	78Q2120 Pin Name	NetPHY-1LP Pin Name	Comments
1	PCSBP	PCSBP	
2	ISODEF	ISODEF	
3	ISO	ISO	
4	GND	TGND	
5	CKIN	REFCLK	
6	No Connect	CLK25	This output from the NetPHY-1LP device provides a 25-MHz clock to the MAC when the CLK25EN pin is pulled low.
7	GND	BURN_IN	When pulled high, this NetPHY-1LP input places the device in Burn-in mode. Left unconnected or pulled low, the device operates normally.
8	RST	RST	
9	PWRDN	PWRDN	
10	VCC	PLLVCC	
11	GND	PLLGND	
12	GND	OGND1	
13	VCC	OVDD1	
14	PHYAD4	PHYAD[4]/10RXD-	Certain MACs (DEC 21143) provide a 5B Symbol serial 10BASE-T interface. The PHYAD[4:0] implements this interface when PCSBP is high. Resistors in the range of of 1 kΩ to 4.7 kΩ shuould be used to set all PHYAD pins.
15	PHYAD3	PHYAD[3]/10RXD+	When PCSBP is high, this pin is used for the 5B Symbol interface.
16	PHYAD2	PHYAD[2]/10TXD++	When PCSBP is high, this pin is used for the 5B Symbol interface.
17	PHYAD1	PHYAD[1]/10TXD+	When PCSBP is high, this pin is used for the 5B Symbol interface.
18	PHYAD0	PHYAD[0]/10TXD-	When PCSBP is high, this pin is used for the 5B Symbol interface.
19	GPIO0	GPIO[0]/10TXD--/ 7Wire	When PCSBP is high, this pin is used for the 5B Symbol interface. This pin is used as an input at the rising edge of RST. If this pin is pulled low through a 10-kΩ resistor during reset, the GPSI 7-wire interface is enabled for 10BASE-T. If this pin is left unconnected during reset, the standard MII mode is enabled.
20	GPIO1	GPIO[1]/TP125	This pin is used as an input at the rising edge of RST. If this pin is pulled high through a 10-kΩ resistor during reset, the NetPHY-1LP device is configured to use a 1.25:1 transformer. If this pin is left unconnected during reset, the NetPHY-1LP device is configured to use a 1:1 transformer.
21	MDIO	MDIO	

Pin Number	78Q2120 Pin Name	NetPHY-1LP Pin Name	Comments
22	MDC	MDC	
23	RXD3	RXD[3]	
24	RXD2	RXD[2]	
25	RXD1	RXD[1]	
26	RXD0	RXD[0]/10RXD	This pin provides the 10-MHz serial-data output when the 7-wire GPSI mode is selected.
27	VCC	VDD1	
28	GND	DGND	
29	RX_DV	RX_DV	
30	RX_CLK	RX_CLK/10RXCLK	This pin provides the 10-MHz receive-clock output when the 7-wire GPSI mode is selected.
31	RX_ER	RX_ER/RXD[4]	When PCSBP is high, this pin is used for the 5B Symbol interface.
32	TX_ER	TX_ER/TXD[4]	When PCSBP is high, this pin is used for the 5B Symbol interface.
33	TX_CLK	TX_CLK/ 10TXCLK/ PCSB_CLK	This output pin provides the 10-MHz transmit clock when the NetPHY-1LP device is operating in the GPSI mode. In the PCS bypass mode, this pin provides the 25-MHz clock for 100BASE-TX operation or the 20-MHz clock for 10BASE-T operation.
34	TX_EN	TX_EN/10TXEN	This pin is the transmit enable when operating in the 7-wire GPSI mode.
35	GND	DGND	
36	VCC	VDD2	
37	TXD0	TXD[0]/10TXD	This pin is used as the 10-MHz serial data input when the 7-wire GPSI mode is selected.
38	TXD1	TXD[1]	
39	TXD2	TXD[2]	
40	TXD3	TXD[3]	
41	COL	COL/10COL	In the GPSI 7-wire mode of operation, this pin indicates a collision.
42	CRS	CRS/10CRS	In the GPSI 7-wire mode of operation, this pin indicates carrier sense.
43	INTR	INTR	

Pin Number	78Q2120 Pin Name	NetPHY-1LP Pin Name	Comments
44	LEDBTX	LEDSPD[0]/ LEDBTA/ FX_SEL	In the standard LED configuration, this pin functions identically on both devices, indicating the 100BASE-TX link status. In the advanced LED configuration, this LED provides an indication of the 10BASE-T link status and activity. This pin is also used as an input during reset. At the rising edge of RST, if this pin is pulled low through a 1-kΩ resistor, the NetPHY-1LP device will be configured for 100BASE-FX operation. If this pin is not pulled down, the device will be configured for 100BASE-TX or 10BASE-T operation.
45	LEDCOL	LEDCOL/ SCRAM_EN	When this pin is pulled low through a 1-kΩ resistor at the rising edge of RST, the scrambler/descrambler will be disabled. If this pin is not pulled down during reset, the scrambler/descrambler will be enabled.
46	LEDRX	LEDRX/LEDSEL	When this pin is pulled low through a 2.5-kΩ resistor at the rising edge of RST, the advanced LED configuration will be selected. If this pin is not pulled down, the standard LED configuration will be selected.
47	LEDTX	LEDTX/LEDBTB	In the standard LED configuration, this pin functions identically on both devices, indicating the 10BASE-T transmit status. In the advanced LED configuration, this LED provides an indication of the 10BASE-T link status and activity.
48	LEDL	LEDNK/ LED_10LNK/ LED_PCSB_SD	This pin indicates the 10BASE-T link status, when operating in the 7-wire GPSI mode. In the PCS bypass mode, this pin indicates signal detect. In MII mode, the signal is active low; it is active high in PSCBP mode.
49	VCC	OVDD2	
50	GND	OGND2	
51	GND	CRVGND	
52	VCC	CRVVCC	
53	TECH2	TECH_SEL[2]	
54	TECH1	TECH_SEL[1]	
55	TECH0	TECH_SEL[0]	
56	ANEGA	ANEGA	
57	LEDBT	LEDSPD[1]/ LEDTXA/ CLK25EN	In the standard LED configuration, this pin functions identically on both devices, indicating the 10BASE-T link status. In the advanced LED configuration, this LED provides an indication of the 100BASE-TX link status and activity. This pin is also used as an input during reset. At the rising edge of RST, if this pin is pulled low through a 1-kΩ resistor, the NetPHY-1LP device will output a 25-MHz clock on the CLK25 pin. If this pin is not pulled down, the CLK25 pin will not be active.
58	LEDFDX	LEDDPX/LEDTXB	In the standard LED configuration, this pin functions identically on both devices, indicating the duplex link status. In the advanced LED configuration, this LED provides an indication of the 100BASE-TX link status and activity.

Pin Number	78Q2120 Pin Name	NetPHY-1LP Pin Name	Comments
59	VCC	ADPVCC	
60	VCC	EQVCC	
61	RPTR	RPTR	
62	NC	TEST3/SDI+	In the 100BASE-FX mode of operation, this input will be high when the received signal quality is good.
63	RXIN	RX-	
64	RXIP	RX+	
65	GND	EQGND	
66	No Connect	TEST0/FXR-	This pin is an output, monitoring the internal test, during Burn-in operation. In the 100BASE-FX mode of operation, this pin is the PECL negative receive input.
67	No Connect	TEST1/FXR+	This pin is an output, monitoring the internal test, during Burn-in operation. In the 100BASE-FX mode of operation, this pin is the PECL positive receive input.
68	No Connect	TEST2	This pin is an output, monitoring the internal test, during Burn-in operation.
69	No Connect	FXT+	In the 100BASE-FX mode of operation, this pin is the PECL positive-transmit output.
70	RIBB_RET	FXT-	The NetPHY-1LP device does not ground the Pin 72 resistor via this pin. In the 100BASE-FX mode of operation, this pin is the PECL negative-transmit output. This pin is a No Connect in other modes.
71	GND	REFGND	
72	RIBB	IBREF	This pin should be connected to analog ground through a 10.0-kΩ 1% resistor.
73	VCC	REFVCC	
74	XTLN	XTL-	
75	XTLP	XTL+	
76	GND	TGND2	
77	TXOP	TX+	
78	TXON	TX-	
79	VCC	TVCC1	
80	VCC	TVCC2	
60	VCC	EQVCC	

Management Registers

The management registers of the NetPHY-1LP device are identical to those of the 78Q2120, with the following exceptions:

1. In the Auto-Negotiation Advertisement Register (MR4), bit 14 is reserved in the 78Q2120. This bit provides an acknowledgement indication in the NetPHY-1LP device, after three consecutive and consistent FLP bursts are received.
2. The Auto-Negotiation Link Partner Ability Register (MR5) provides an additional Next Page format that is not available in the 78Q2120. See the NetPHY-1LP data sheet for details.

3. In the Auto-Negotiation Expansion Register (MR6), bit 2 is permanently set to zero in the 78Q2120 to indicate that the Next Page function is not supported. This bit is permanently set to one in the NetPHY-1LP device to indicate that this function is supported.
4. The Auto-Negotiation Next Page Advertisement register (MR7) does not exist in the 78Q2120. The NetPHY-1LP device includes this register to send the Next Page message. See the NetPHY-1LP data sheet for details.
5. The 78Q2120 includes a transmit-high impedance function, controlled by bit 12 of the Miscellaneous Features Register (or Vendor Specific Register) (MR16). This bit is reserved in the NetPHY-1LP device. Similarly, the 78Q2120 uses bit one of this register to control the PCS Bypass function. The NetPHY-1LP device uses bit 1 of MR21 to control the PCS Bypass function.
6. In the Interrupt Control/Status register (MR17), bits 10 and 2 are slightly different in the 78Q2120 and the NetPHY-1LP device. In the 78Q2120, these bits are used to enable and indicate an interrupt for any change of the link state. In the NetPHY-1LP device, these bits are used to enable and indicate an interrupt only when the link state changes from OK to either Fail or Ready.
7. In the Diagnostic register (MR18), bit 12 indicates that Auto-Negotiation has failed in the 78Q2120. This bit is reserved in the NetPHY-1LP device.
8. The following registers do not have equivalents in the 78Q2120 (see the NetPHY-1LP data sheet for details):
   a. Power/Loopback Register (MR19)
   b. Mode Control Register (MR21)
   c. Disconnect Counter (MR23)
   d. Receive Error Counter (MR24)

Additional Functions of the NetPHY-1LP Device

The NetPHY-1LP device provides five significant enhanced functions, beyond those of the TDK 78Q2120. These functions are 100BASE-FX operation, 7-wire General Purpose Serial Interface (GPSI) for 10BASE-T operation, 5B Symbol MAC interface, enhanced LED operation, and operation with a 1.25:1 transformer.

100BASE-FX Operation

The 100BASE-FX operation is selected by pulling the LEDSPD[0]/LEDBTB/FX_SEL input low through a 1-kΩ resistor. This enables the 100BASE-FX functions of the TEST0/FXR-, TEST1/FXR+, FXT-, FXT+, and TEST3/SDI+ pins.

For 100BASE-FX operation, the resistive termination must be changed. When a 3.3-V fiber-optic transceiver is used, follow the recommended termination shown in the Am79C874 NetPHY-1LP data sheet. Note that fiber-optic transceiver vendors may have different recommendations for receive-pair termination on their side of the receive-pair capacitors.

When a 5-V fiber-optic transceiver is used, it may be possible to eliminate the receive-pair capacitors and the termination resistors on the fiber-optic transceiver side. The transmit-pair should be terminated via 82-Ω resistors to 5 V and 130-Ω resistors to ground. The NetPHY-1LP device SDI+ pin should have a 301-Ω resistor to ground and a 200-Ω series resistor between 301-Ω resistor and the SD pin on the fiber-optic transceiver.

7-Wire GPSI MAC Interface

7-Wire GPSI operation of the NetPHY-1LP device is selected when the GPIO[0]/10TXD--/7Wire pin is pulled to ground through a 10-kΩ resistor. This enables the GPSI MAC interface on the RXD[0]/10RXD, RX_CLK/10RXCLK, TX_CLK/10TXCLK/PCSBP_CLK, TX_EN/10TXEN, TXD[0]/10TXD, COL/10COL, and CRS/10CRS pins. In this mode, the NetPHY-1LP device may be used with MACs that implement the GPSI, such as the Motorola QUICC™ and PowerQUICC™ microprocessors.

5B Symbol MAC Interface

The NetPHY-1LP device provides a serial-differential interface for use with the Intel/DEC 21143 MAC in the internal SIA (10BASE-T) mode. In this mode, the NetPHY-1LP device operates as a 10BASE-T transceiver, providing received data to the 21143 over a serial-differential pair. The 21143 uses two serial-differential pairs to provide transmit data to the NetPHY-1LP device, where the two differential pairs are combined in the NetPHY-1LP device to compensate for inter-symbol interference on the twisted-pair medium.

Advanced LED Functions

The NetPHY-1LP device provides advanced LED functions when the LEDRX/LEDSEL pin is pulled low through a 2.5-kΩ resistor. Two dual-color LEDs are used in this mode to indicate transmit and receive activity, duplex status, and speed of a link using only four pins.

1.25:1 Transformer

When the GPIO[1]/TP125 pin is pulled high through a 10-kΩ resistor, twisted-pair operation with a 1.25:1 transformer is selected. In this mode, the transmit section of the NetPHY-1LP device dissipates 20% less power when operating, resulting in a 10% overall reduction of power dissipation. When this mode is se-

lected, the transmit-termination resistors must be changed to 78.1-Ω 1% resistors.

Passive Components

The passive components used by both the 78Q2120 and the NetPHY-1LP device for series termination of the MII, pull-up of LEDs, and termination of the twisted-pair signals when using a 1:1 transformer are the same. The bias resistor, connected to RIBB and RIBB_RET of the 78Q2120 and IBREF of the NetPHY-1LP device, is a 10.0-kΩ 1% resistor, rather than the 9.76 kΩ 1% resistor as when the 78Q2120 is operating at 3.3 V.

Finally, if the default configuration provided by the NetPHY-1LP device pins is desired, many of the configuration pins may be left unconnected. Where the configuration pins of the 78Q2120 must be connected to power or ground, either directly or through a resistor, the NetPHY-1LP device includes internal resistors on the configuration inputs to allow the designer to leave these pins unconnected when selecting the default function of the pin. The pins with internal resistors are shown in Table 3.

Table 3. NetPHY-1LP Pins with Internal Resistors

Pin	Name	Resistor	Function
1	PCSBP	Pull down	Disables the PCS bypass function.
2	ISODEF	Pull down	Enables the MII output pins by default.
3	ISO	Pull down	Enables the MII output pins.
7	BURN_IN	Pull down	Burn-in test is disabled.
8	RST	Pull up	Disables reset.
9	PWRDN	Pull down	Normal operation is selected.
14	PHYAD[4]	Pull up	PHYAD[4] = 1
15	PHYAD[3]	Pull up	PHYAD[3] = 1
16	PHYAD[2]	Pull up	PHYAD[2] = 1
17	PHYAD[1]	Pull up	PHYAD[1] = 1
18	PHYAD[0]	Pull up	PHYAD[0] = 1
19	GPIO[0]	Pull up	Standard MII operation is selected at reset.
20	GPIO[1]	Pull down	1:1 transformer operation is selected at reset.
21	MDIO	Pull down	Requires only external 1.5-kΩ pull up.
44	LEDSPD[0]	Pull up	100BASE-TX operation is selected at reset.
45	LEDCOL	Pull up	Scrambler operation is enabled at reset.
46	LEDRX	Pull up	Standard LED operation is selected at reset.
53	TECH_SEL[2]	Pull up	TECH_SEL[2] = 1
54	TECH_SEL[1]	Pull up	TECH_SEL[1] = 1
55	TECH_SEL[0]	Pull up	TECH_SEL[0] = 1
56	ANEGA	Pull up	Auto-Negotiation is enabled at reset.
57	LEDSPD[1]	Pull up	Disables 25-MHz clock output on CLK25 pin at reset.

Note: *The default values for the TECH_SEL[2:0] inputs cause the NetPHY-1LP device to advertise all capabilities during Auto-Negotiation.*

REVISION SUMMARY

Revisions to other versions this document are as follows:

Revision A to B

1. Pins 14-18: Specified using resistors in the range of 1 kΩ to 4.7 kΩ for setting PHYAD pins.
2. Pin 48: Added note on signal level.

Trademarks

AMD, the AMD logo, and combinations thereof, and NetPHY are trademarks of Advanced Micro Devices, Inc.

PowerQUICC and QUICC are trademarks of Motorola, Inc.

Other product names used in this publication are for identification purposes only and may be trademarks of their respective companies.