

**3.3 V 168-pin Registered SDRAM Modules  
256 MB, 512 MB & 1 GB Densities**

- 168-pin JEDEC Standard, Registered 8 Byte Dual-In-Line SDRAM Modules for Server main memory applications using memory frequencies up to 100MHz
- One bank 32M × 72 and 64M × 72 organization, two bank 128M × 72 organization
- Optimized for ECC applications with very low input capacitances
- Programmed Latencies:
 

CL	$t_{RCD}$	$t_{RP}$
2	2	2
- Single + 3.3 V (± 0.3 V) power supply

- Programmable  $\overline{CAS}$  Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All inputs and outputs are LVTTTL compatible
- Serial Presence Detect with E<sup>2</sup>PROM
- Utilizes SDRAMs in TSOPII-54 packages with registers and PLL. The two bank module uses stacked TSOP54 packages.
- Card Size: 133.35 mm × 43.18 mm with Gold contact pads (JEDEC MO-161)
- These Registered DIMM modules support operation in “registered” and “buffered” mode

• Performance:

		-8		Unit
		registered	buffered	
$f_{CK}$	Clock Frequency (max.)	100	66	MHz
$t_{CK}$	Clock Cycle Time (min.)	10	15	ns
$t_{AC}$	Clock Access Time (max.)	6	6	ns

The HYS 72Vx3xxGR-8 family are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) which are organized as 32M × 72, 64M × 72 & 128M × 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for ECC applications. All control and address signals are registered on-DIMM and the design incorporates a PLL circuit for the Clock inputs. Use of an on-board register reduces capacitive loading on the input signals but are delayed by one cycle in arriving at the SDRAM devices. Decoupling capacitors are mounted on the PC board. The DIMMs use a serial presence detects scheme implemented via a serial E<sup>2</sup>PROM using the 2-pin I<sup>2</sup>C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint. The PCB layout is based on latest industry PC133/PC100 standard gerber files. Besides standard PC100 applications, this module family is intended for applications where Registered DIMM modules are used in “buffered mode” at a 67 MHz memory bus speed.

**Ordering Information**

<b>Type</b>	<b>Compliance Code</b>	<b>Description</b>	<b>SDRAM Components</b>
HYS 72V32301GR-8	PC100-222-622R	one bank 256 MB Reg. DIMM	128 MBit (x4) HYB39S128400CT-7.5 with trp<= 15ns
HYS 72V64300GR-8	PC100-222-622R	one bank 512 MB Reg. DIMM	256 MBit (x4) HYB39S256400CT-7.5 with trp<= 15ns
HYS 72V128320GR-8	PC100-222-622R	two bank 1 GByte Reg. DIMM	256 MBit (x4 stacked) HYB39S256400CT-7.5 with trp<= 15ns

*Note: All part numbers end with a place code (not shown), designating the die revision. Consult factory for current revisions. Example: HYS 72V64300GR-8-C2, indicating Rev. C2 dies are used for SDRAM components.*

### Pin Definitions and Functions

A0 - A11, A12	Address Inputs	DQMB0 - DQMB7	Data Mask
BA0, BA1	Bank Selects	$\overline{CS0} - \overline{CS3}$	Chip Select
DQ0 - DQ63	Data Input/Output	REGE *)	Register Enable "H" or N.C = registered mode "L" = buffered mode
CB0 - CB7	Check Bits (x72 organization only)	$V_{DD}$	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	$V_{SS}$	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read/Write Input	SDA	Serial Data Out
CKE0	Clock Enable	N.C.	No Connection
CLK0 - CLK3	Clock Input	-	-

\*) note : both operation modes are supported by this module family

### Address Format

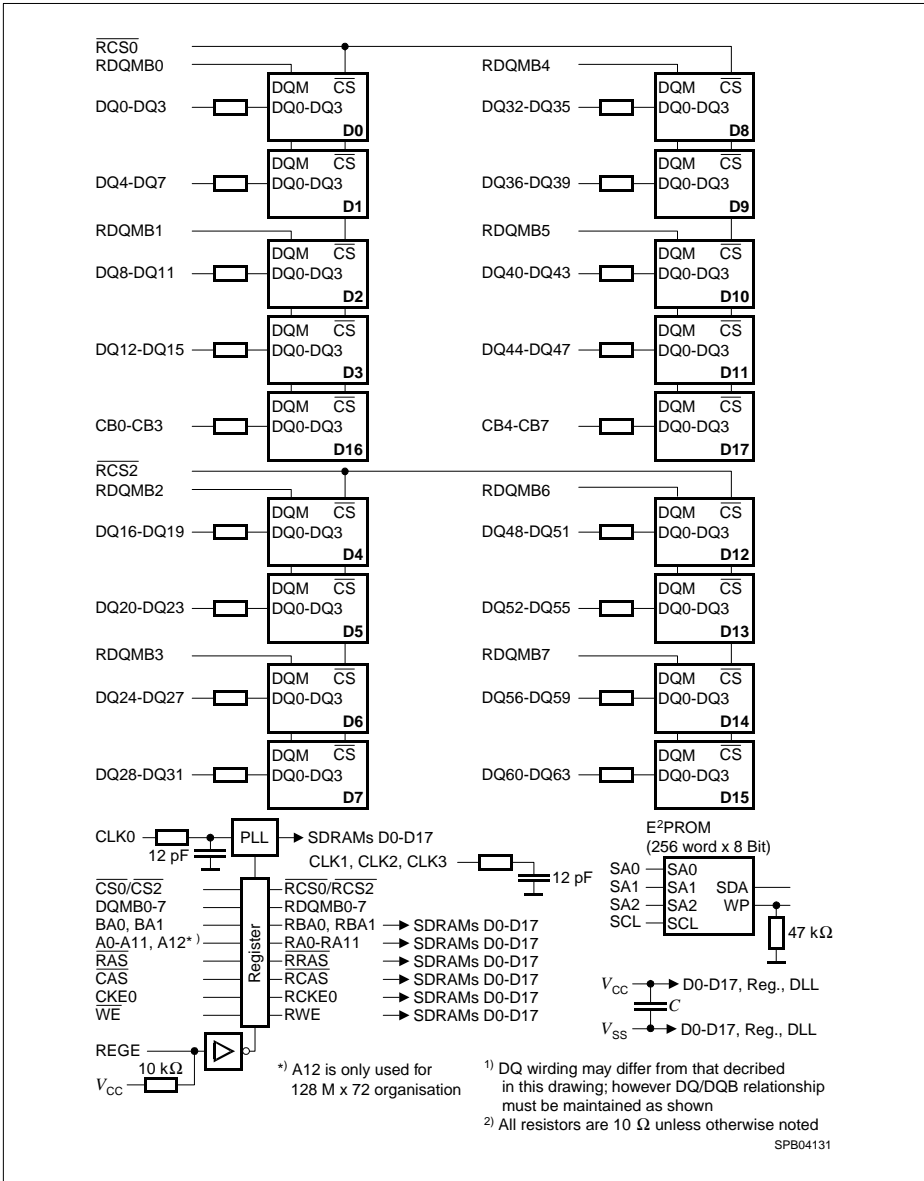
Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
256 MB	32M × 72	1	32M × 4	18	12/2/11	4k	64 ms	15.6 μs
512 MB	64M × 72	1	64M × 4	18	13/2/11	8k	64 ms	7.8 μs
1 GB	128M × 72	2	64M × 4	36	13/2/11	8k	64 ms	7.8 μs

### Pin Configuration

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
1	$V_{SS}$	43	$V_{SS}$	85	$V_{SS}$	127	$V_{SS}$
2	DQ0	44	DU	86	DQ32	128	CKE0
3	DQ1	45	$\overline{CS2}$	87	DQ33	129	$\overline{CS3}$
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	$V_{DD}$	48	DU	90	$V_{DD}$	132	N.C.
7	DQ4	49	$V_{DD}$	91	DQ36	133	$V_{DD}$
8	DQ5	50	N.C.	92	DQ37	134	N.C.
9	DQ6	51	N.C.	93	DQ38	135	N.C.
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	$V_{SS}$	54	$V_{SS}$	96	$V_{SS}$	138	$V_{SS}$
13	DQ9	55	DQ16	97	DQ41	139	DQ48

**Pin Configuration (cont'd)**

PIN#	Symbol	PIN#	Symbol	PIN#	Symbol	PIN#	Symbol
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V <sub>DD</sub>	101	DQ45	143	V <sub>DD</sub>
18	V <sub>DD</sub>	60	DQ20	102	V <sub>DD</sub>	144	DQ52
19	DQ14	61	N.C.	103	DQ46	145	N.C.
20	DQ15	62	DU	104	DQ47	146	DU
21	CB0	63	N.C.	105	CB4	147	REGE
22	CB1	64	V <sub>SS</sub>	106	CB5	148	V <sub>SS</sub>
23	V <sub>SS</sub>	65	DQ21	107	V <sub>SS</sub>	149	DQ53
24	N.C.	66	DQ22	108	N.C.	150	DQ54
25	N.C.	67	DQ23	109	N.C.	151	DQ55
26	V <sub>DD</sub>	68	V <sub>SS</sub>	110	V <sub>DD</sub>	152	V <sub>SS</sub>
27	$\overline{WE}$	69	DQ24	111	$\overline{CAS}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{CS0}$	72	DQ27	114	$\overline{CS1}$	156	DQ59
31	DU	73	V <sub>DD</sub>	115	$\overline{RAS}$	157	V <sub>DD</sub>
32	V <sub>SS</sub>	74	DQ28	116	V <sub>SS</sub>	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V <sub>SS</sub>	120	A7	162	V <sub>SS</sub>
37	A8	79	CLK2	121	A9	163	CLK3
38	A10 (AP)	80	N.C.	122	BA0	164	N.C.
39	BA1	81	WP	123	A11	165	SA0
40	V <sub>DD</sub>	82	SDA	124	V <sub>DD</sub>	166	SA1
41	V <sub>DD</sub>	83	SCL	125	CLK1	167	SA2
42	CLK0	84	V <sub>DD</sub>	126	A12	168	V <sub>DD</sub>





### Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to $V_{SS}$	$V_{IN}, V_{OUT}$	- 1.0	4.6	V
Power supply voltage on $V_{DD}$ to $V_{SS}$	$V_{DD}$	- 1.0	4.6	V
Storage temperature range	$T_{STG}$	-55	+150	°C
Power dissipation (per SDRAM component)	$P_D$	-	1	W
Data out current (short circuit)	$I_{OS}$	-	50	mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.  
Functional operation should be restricted to recommended operation conditions.  
Exposure to higher than recommended voltage for extended periods of time affect device reliability

### DC Characteristics

$T_A = 0$  to  $70$  °C<sup>1)</sup>;  $V_{SS} = 0$  V;  $V_{DD} = 3.3$  V  $\pm$  0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	$V_{IH}$	2.0	$V_{DD} + 0.3$	V
Input Low Voltage	$V_{IL}$	- 0.5	0.8	V
Output High Voltage ( $I_{OUT} = - 4.0$ mA)	$V_{OH}$	2.4	-	V
Output Low Voltage ( $I_{OUT} = 4.0$ mA)	$V_{OL}$	-	0.4	V
Input Leakage Current, any input ( $0$ V < $V_{IN} < 3.6$ V, all other inputs = $0$ V)	$I_{I(L)}$	- 10	10	$\mu$ A
Output Leakage Current (DQ is disabled, $0$ V < $V_{OUT} < V_{DD}$ )	$I_{O(L)}$	- 10	10	$\mu$ A

### Capacitance

$T_A = 0$  to  $70$  °C<sup>1)</sup>;  $V_{DD} = 3.3$  V  $\pm$  0.3 V,  $f = 1$  MHz

Parameter	Symbol	Limit Values		Unit
		One Bank Modules	Two Bank Modules	
Input Capacitance (all inputs except CLK and CKE)	$C_{IN}$	10	20	pF
Input Capacitance (CLK)	$C_{CLK}$	30	30	pF
Input Capacitance (CKE)	$C_{CKE}$	17	30	pF
Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	$C_{IO}$	10	17	pF
Input Capacitance (SCL, SA0 - 2)	$C_{SC}$	8	8	pF
Input/Output Capacitance (SDA)	$C_{SD}$	8	8	pF

**Operating Currents per SDRAM component**

$T_A = 0$  to  $70\text{ °C}$  <sup>1)</sup>,  $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$

(Recommended Operating Conditions unless otherwise noted)

Parameter	Test Condition	Symbol	128Mb	256Mb	Unit	Note
			max.	max.		
Operating current  $t_{RC} = t_{RC(MIN.)}$ , $t_{CK} = t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL = 3. All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	–	$I_{CC1}$	150	210	mA	2)
Precharge stand-by current in Power Down Mode $\overline{CS} = V_{IH(MIN.)}$ , $CKE \leq V_{IL(MAX.)}$	$t_{CK} = \text{min.}$	$I_{CC2P}$	2	2		
No operating current  $t_{CK} = \text{min.}$ , $\overline{CS} = V_{IH(MIN.)}$ , active state (max. 4 banks)	$CKE \geq V_{IH(MIN.)}$	$I_{CC3N}$	45	45	mA	2)
	$CKE \leq V_{IL(MAX.)}$	$I_{CC3P}$	10	10	mA	2)
Burst operating current  $t_{CK} = \text{min.}$ , Read command cycling	–	$I_{CC4}$	90	120	mA	2), 3)
Auto refresh current  $t_{CK} = \text{min.}$ , Auto Refresh command cycling	–	$I_{CC5}$	210	240	mA	2)
Self refresh current Self Refresh Mode, $CKE = 0.2\text{ V}$	–	$I_{CC6}$	1.5	2.5	mA	2)

**AC Characteristics (SDRAM Device Specification)** <sup>4), 5)</sup>

$T_A = 0$  to  $70$  °C <sup>1)</sup>;  $V_{SS} = 0$  V;  $V_{DD} = 3.3$  V  $\pm$  0.3 V,  $t_T = 1$  ns

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		

**Clock and Access Times**

Clock Cycle Time CAS Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$t_{CK}$	10	–	ns	8)
		10	–	ns	
Clock Frequency CAS Latency = 3 $\overline{\text{CAS}}$ Latency = 2	$f_{CK}$	–	100	MHz	8)
		–	100	MHz	
Access Time from Clock CAS Latency = 3 CAS Latency = 2	$t_{AC}$	–	6	ns	–
		–	6	ns	
Clock High Pulse Width	$t_{CH}$	3	–	ns	–
Clock Low Pulse Width	$t_{CL}$	3	–	ns	–
Transition Time	$t_T$	0.5	10	ns	–

**Setup and Hold Parameters**

Input Setup Time	$t_{IS}$	2	–	ns	–
Input Hold Time	$t_{IH}$	1	–	ns	–
Power Down Mode Entry Time	$t_{SB}$	–	1	CLK	–
Power Down Mode Exit Setup Time	$t_{PDE}$	1	–	CLK	–
Mode Register Set-up Time	$t_{RSC}$	2	–	CLK	–
Transition Time	$t_T$	0.5	10	ns	–

**Common Parameters**

Row to Column Delay Time	$t_{RCD}$	20	–	ns	–
Row Precharge Time	$t_{RP}$	15	–	ns	8)
Row Active Time	$t_{RAS}$	50	100k	ns	–
Row Cycle Time	$t_{RC}$	70	–	ns	–
Activate (a) to Activate (b) Command Period	$t_{RRD}$	2	–	CLK	–
$\overline{\text{CAS}}$ (a) to $\overline{\text{CAS}}$ (b) Command Period	$t_{CCD}$	1	–	CLK	–

**AC Characteristics (SDRAM Device Specification)** (cont'd) <sup>4), 5)</sup>

$T_A = 0$  to  $70$  °C <sup>1)</sup>;  $V_{SS} = 0$  V;  $V_{DD} = 3.3$  V  $\pm$  0.3 V,  $t_T = 1$  ns

Parameter	Symbol	Limit Values		Unit	Note
		min.	max.		

**Refresh Cycle**

Refresh Period (128 Mb components)	$t_{REF}$	–	15.6	$\mu$ s	–
Refresh Period (256 Mb components)	$t_{REF}$	–	7.8	$\mu$ s	–
Self Refresh Exit Time	$t_{SREX}$	1	–	CLK	<sup>6)</sup>

**Read Cycle**

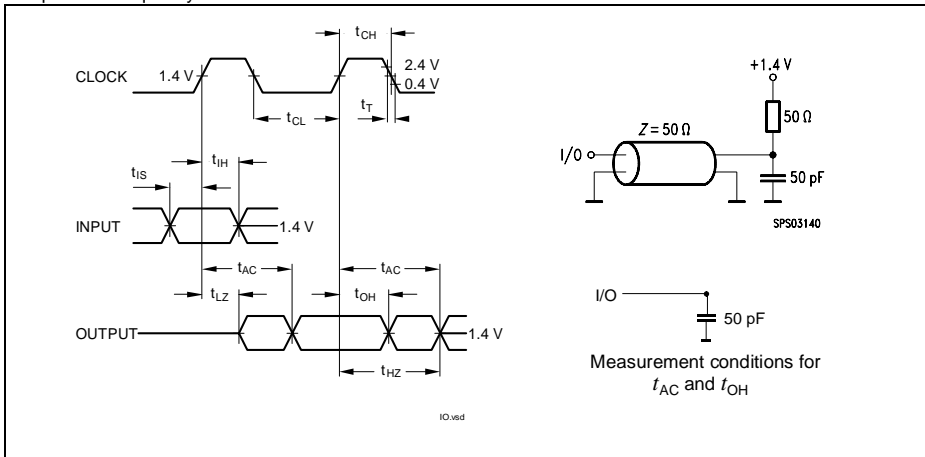
Data Out Hold Time	$t_{OH}$	3	–	ns	–
Data Out to Low Impedance	$t_{LZ}$	0	–	ns	<sup>7)</sup>
Data Out to High Impedance	$t_{HZ}$	3	8	ns	<sup>7)</sup>
DQM Data Out Disable Latency	$t_{DQZ}$	–	2	CLK	–

**Write Cycle**

Data Input to Precharge (write recovery)	$t_{WR}$	2	–	CLK	<sup>8)</sup>
DQM Write Mask Latency	$t_{DQW}$	0	–	CLK	–

**Notes**

1. The registered DIMM modules are designed to operate under system operating conditions between 0-55 deg C ambient, 500 MB/sec sustained bandwidth and 0 LFM airflow. Operating at higher ambient temperatures needs sufficient air flow to limit the case temperature of the SDRAM components do not exceed 85°C. Maximum operation frequency of this module family is 100MHz when operating in "registered mode" and 67 MHz when in "buffered mode"
2. These parameters depend on the cycle rate. All values are measured at 100MHz operation frequency. Input signals are changed once during tck excepts for lcc6 and for standby currents when tck = infinity.
3. These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the data-out current is excluded.
4. An initial pause of 100 µs is required after power-up. Then a Precharge All Banks command must be given followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin. Also the on-DIMM PLL must be given enough clock cycles to stabilize before any operation can be guaranteed.
5. AC timing tests have  $V_{IL} = 0.8\text{ V}$  and  $V_{IH} = 2.0\text{ V}$  with the timing referenced to the 1.4 V crossover point. The transition time is measured between  $V_{IH}$  and  $V_{IL}$ . All AC measurements assume  $t_T = 1\text{ ns}$  with the AC output load circuit shown. Specified  $t_{AC}$  and  $t_{OH}$  parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
6. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to  $t_{RC}$  is satisfied after the Self Refresh Exit command is registered.
7. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.
8. This module family uses SDRAM components with a write recovery time  $t_{wr}$  (sometimes also named  $tdp1$ ) of two clocks and a  $t_{rp}$  ("precharge time") of  $\leq 15\text{ ns}$  to achieve proper operation in "buffered mode" at a operation frequency of 67 MHz.



**Serial Presence Detect**

A serial presence detect storage device - E<sup>2</sup>PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E<sup>2</sup>PROM device during module production using a serial presence detect protocol (I<sup>2</sup>C synchronous 2-wire bus)

**SPD-Table for Registered DIMM Modules**

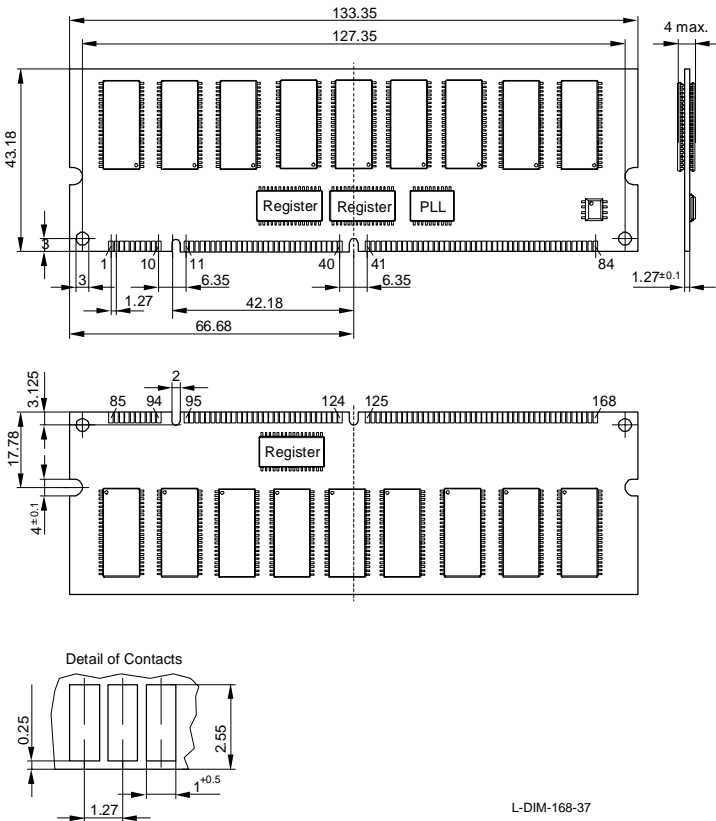
Byte#	Description	SPD Entry Value	Hex		
			256 MB 1 Bank-	512 MB 1 Bank	1 GB 2 Banks
0	Number of SPD Bytes	128	80		
1	Total Bytes in Serial PD	256	08		
2	Memory Type	SDRAM	04		
3	Number of Row Addresses (without BS bits)	12/13	0C	0D	0D
4	Number of Column Addresses	11	0B	0B	0B
5	Number of DIMM Banks	1	01	01	02
6	Module Data Width	72	48		
7	Module Data Width (cont'd)	0	00		
8	Module Interface Levels	LVTTL	01		
9	Cycle Time at CL = 3	10.0 ns	A0		
10	Access Time from Clock at CL = 3	6.0 ns	60		
11	DIMM Config (Error Det/Corr.)	ECC	02		
12	Refresh Rate/Type	Self-Refresh, 15.6 / 7.8 $\mu$ s	80	82	82
13	SDRAM Width, Primary	x4	04		
14	Error Checking SDRAM Data Width	x4	04		
15	Minimum $t_{CCD}$	1 CLK	01		
16	Burst Length Supported	1, 2, 4, 8	0F		
17	Number of SDRAM Banks	4	04		
18	SDRAM Supported CAS Latencies	2 & 3	06		
19	SDRAM CS Latencies	0	01		
20	SDRAM WE Latencies	0	01		
21	SDRAM DIMM Module Attributes	registered/buffered	1F		
22	SDRAM Device Attributes	$V_{DD}$ tol +/- 10%	0E		
23	Min. Clock Cycle Time at CL = 2	10 ns	A0		
24	Max. Data Access Time from Clock for CL = 2	6 ns	60		
25	Min. Clock Cycle Time at CL = 1	not supp.	00		
26	Max. Data Access Time from Clock at CL = 1	not supp.	00		
27	SDRAM Minimum $t_{RP}$	15 ns	0F		
28	SDRAM Minimum $t_{RRD}$	20 ns	14		
29	SDRAM Minimum $t_{RCD}$	20 ns	14		
30	SDRAM Minimum $t_{RAS}$	50 ns	32		
31	Module Bank Density (per bank)	256/ 512 MByte	40	80	80
32	SDRAM Input Setup Time	2 ns	20		
33	SDRAM Input Hold Time	1 ns	10		

**SPD-Table for Registered DIMM Modules** (cont'd)

Byte#	Description	SPD Entry Value	Hex		
			256 MB 1 Bank-	512 MB 1 Bank	1 GB 2 Banks
34	SDRAM Data Input Setup Time	2 ns	20		
35	SDRAM Data Input Hold Time	1 ns	10		
36-61	Superset Information (may be used in future)	–	00		
62	SPD Revision	1.2	12		
63	Checksum for Bytes 0 - 62	–	DB	1E	1F
64-125	Manufacturer's Information	–	XX		
126	Frequency Specification	100MHz	64		
127	Details of Clocks	–	8F		
128+	Unused Storage Locations	–	FF		

Package Outlines

**Module Package**  
**JEDEC MO-161**  
**256 & 512 MByte Registered Module based**  
**on x4 organised SDRAMs**



note: all tolerances are in accordance with the JEDEC standard



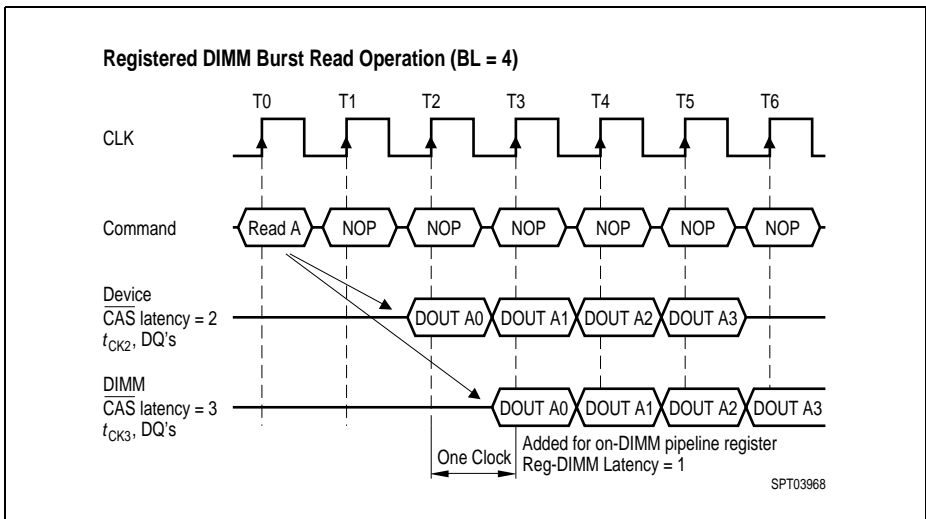
**Functional Description**

These Registered DIMMs achieve high speed data transfer rate up to 100 MHz, when in “registered mode” and up to 67 MHz when in “buffered mode”. The “registered mode” is achieved when the REGE input signal is in “high” state or the pin is not connected. Operation in “buffered mode” (REGE = “low”) needs careful system design to compensate all input signals for the extra delay time of the register components when in “buffered mode”. “Buffered mode” is limited to 67 Mhz operation.

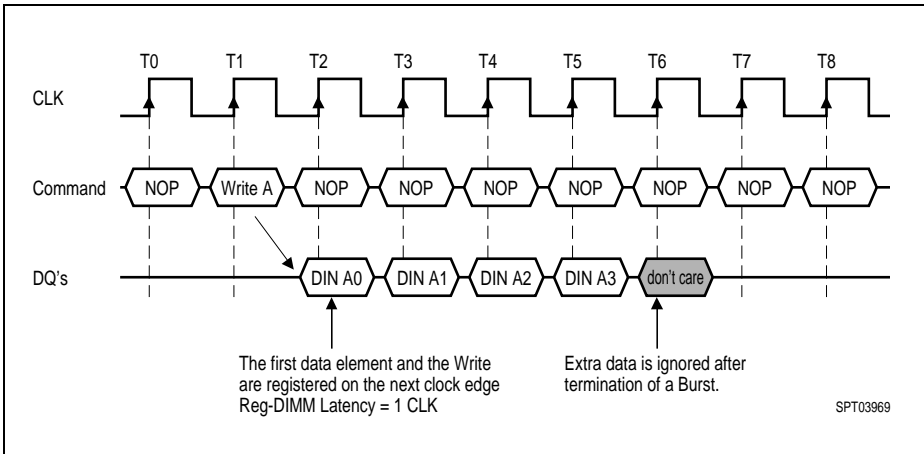
**Registered Mode:**

All control and address signals are synchronized with the positive edge of externally supplied clocks and are registered on-DIMM and hence delayed by one clock cycle in arriving at the SDRAM devices. The use of the on-board register reduces the capacitive loading of the DIMM on input control and address signals. The SDRAM device data lines (DQ) are connected directly to the DIMM tabs through 10 Ohm series resistors. All the following timing diagrams and explanations show DIMM operation at the tabs, not SDRAM operation.

The picture below depicts an overview of the effect of the Registered Mode on the data outputs (DQs) for a Read operation. Without the registers, the data is delayed according to the device  $\overline{\text{CAS}}$  latency, in the case two clocks. With the register, the data is delayed according to the device  $\overline{\text{CAS}}$  latency plus an additional clock cycle. This is known as the DIMM  $\overline{\text{CAS}}$  latency, and in this example is four three. The data path can be thought of as a pipeline in which the register effectively lengthens the pipe by one clock cycle.



In case of a Burst Write Command the data-in is delayed one clock due the op-DIMM pipeline register also. Therefore, data for the first Burst Write cycle must be applied on the DQ pins on the next clock cycle after the Write command is issued. the remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.



Registered DIMM Burst Write Operation (BL = 4)

### Buffered Mode:

Operating margins when Registered DIMM modules are used in “buffered mode” are derived from the post register timing only. For a complete system level timing the system designer must add/ subtract to/from this margin other parameters such as, system to DIMM flight time, clow skew, clock jitter, external register clock to output delay etc.

The table below shows an example for the post register timing for DIMM modules in “buffered mode”:

Property	Time [ns] Set-up	Property	Time [ns] Hold
Tpd.BUF.max	1.96	Tpd.BUF.min	0.91
Tflight.max	3.43	Tflight.min	2.66
Tsso.brd.max	0.30	Tsso.brd.min	0.0
Tsu.SDRAM	2.00	TholdSDRAM	-1.00
Period	15.00		

**tpd.BUF.max:** The maximum time for the signal to exit the register with REGE in a low stgate. This is measured into 0 pf load.

**Tflight.max:** The maximum time for the signal to propagate from the register to the SDRAM

**Tsso.brd.max:** The time the flight time is extended due to simultaneous switching outputs and crosstalk from other signals.

**Tsu.SDRAM:** The set-up required for the SDRAM inputs.

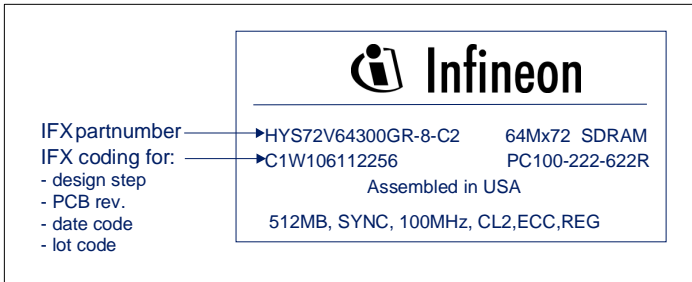
**Tpd.BUF.min. :** The minimum time for the signal to exit the register with REGE in a low state. This is measured into a 0 pf load.

**Tflight.min:** The minimum time for the signal to propagate from the register to the SDRAM

**Thold.DRAM:** The hold time required for the SDRAM inputs

**Period:** Minimum cycle time expressing in ns allowed for operating these Registered DIMM modules in "buffered mode"

**Module Label Example:**



## Rev. Changes

13.2.2001	<p>Target Specification for operation up to 100 MHz in "registered mode" and 67 Mhz when used in "buffered mode"</p> <p>Special module family for applications based on INTEL's 460GX chipset, where PC100 modules are used in "buffered mode" at 67 MHz maximum operation frequency.</p> <p>Uses components with <math>t_{wr} = t_{dpl} = 2 \text{Clock}</math> which support <math>t_{rp} \leq 15\text{ns}</math> to guarantee operation at 67MHz when these modules are used in "buffered mode"</p>
21.6.2001	Outline Drawings updated and changed to L-DIM-168-37 & 37S
29.06.01	Absolute maximum rating section added
06.09.2001	<p>SCR: Thickness of modules with stacked components changed from 6.4 to 6.8 max.</p> <p>Datasheet changed from "Preliminary" to "Final"</p>